IN THE CLAIMS

The claims as pending are submitted herein for the convenience of the Examiner.

1. A packaged semiconductor, comprising:

a semiconductor chip having an upper surface, a perimeter and a bottom surface;

a plurality of input bond pads and output bond pads on said upper surface along said perimeter electrically connected to said semiconductor chip;

a leadframe having a chip paddle, said chip paddle having a top surface, a half-etched section, and a bottom surface, said chip paddle being bonded to said semiconductor chip by an adhesive, said leadframe having a plurality of tie bars, said plurality of tie bars each having a side surface and a bottom surface, each of said plurality of tie bars being connected to said corners of said chip paddle, said plurality of tie bars externally extending from said chip paddle, said leadframe having a plurality of dam bars;

a plurality of leads connected to said leadframe;

a plurality of wires electrically connected to said plurality of leads and said semiconductor chip; and

encapsulation material encapsulating said semiconductor chip, said plurality of conductive wires, said chip paddle, and said plurality of internal leads to form a package body;

wherein said chip paddle has a plurality of through-holes in said half-etched section of said chip paddle for increasing the bonding strength of said encapsulation material in said package body.

2. The packaged semiconductor of claim 1, wherein said chip paddle has a perimeter and said half-etched section is located at a lower edge of said chip paddle along said chip paddle perimeter.

3. The packaged semiconductor of claim 1, wherein said plurality of tie bars each has a side surface and a bottom surface.

4. The packaged semiconductor of claim 1, wherein each of said plurality of tie bars externally extend and has a half-etched section.

5. The packaged semiconductor of claim 1, further comprising a ground ring, said ground ring being electrically connected to said semiconductor chip by said conductive wires.

6. The packaged semiconductor of claim 1, wherein flow of said encapsulation material is limited by said plurality of dam bars formed on said leadframe.

7. The packaged semiconductor of claim 1, wherein said chip paddle has a plurality of tabs in said half-etched section of said chip paddle for increasing the bonding strength of said encapsulation material in said package body.

8. A packaged semiconductor, comprising:

a semiconductor chip having an upper surface, a perimeter and a bottom surface;

a plurality of input bond pads and output bond pads on said upper surface along said perimeter electrically connected to said semiconductor chip;

a leadframe having a chip paddle, said chip paddle having a top surface, a half-etched section, and a bottom surface, said chip paddle being bonded to said semiconductor chip by an adhesive, said leadframe having a plurality of tie bars, said plurality of tie bars each having a side surface and a bottom surface, each of said plurality of tie bars being connected to said corners of said chip paddle, said plurality of tie bars externally extending from said chip paddle, said leadframe having a plurality of dam bars;

a plurality of leads connected to said leadframe;

a plurality of wires electrically connected to said plurality of leads and said semiconductor chip; and

encapsulation material encapsulating said semiconductor chip, said plurality of conductive wires, said chip paddle, and said plurality of internal leads to form a package body;

wherein said chip paddle has a plurality of tabs in said half-etched section of said chip paddle for increasing the bonding strength of said encapsulation material in said package body.

9. The packaged semiconductor of claim 8, wherein said chip paddle has a perimeter and said half-etched section is located at a lower edge of said chip paddle along said chip paddle perimeter.

10. The packaged semiconductor of claim 8, wherein said plurality of tie bars each has a side surface and a bottom surface.

11. The packaged semiconductor of claim 8, wherein each of said plurality of tie bars externally extend and has a half-etched section.

12. The packaged semiconductor of claim 8, further comprising a ground ring, said ground ring being electrically connected to said semiconductor chip by said conductive wires.

13. The packaged semiconductor of claim 8, wherein flow of said encapsulation material is limited by said plurality of dam bars formed on said leadframe.

14. The packaged semiconductor of claim 8, wherein said chip paddle has a plurality of through-holes in said half-etched section of said chip paddle for increasing the bonding strength of said encapsulation material in said package body.

15. A packaged semiconductor, comprising:
a semiconductor chip having an upper surface, a perimeter and a bottom surface;

a plurality of input bond pads and output bond pads on said upper surface along said perimeter electrically connected to said semiconductor chip;

a leadframe having a chip paddle, said chip paddle having a top surface, a half-etched section, and a bottom surface, said chip paddle being bonded to said semiconductor chip by an adhesive, said leadframe having a plurality of tie bars, said plurality of tie bars each having a side surface and a bottom surface, each of said plurality of tie bars being connected to said corners of said chip paddle, said plurality of tie bars externally extending from said chip paddle, said leadframe having a plurality

of dam bars;

a plurality of leads connected to said leadframe;

a plurality of wires electrically connected to said plurality of leads and said semiconductor chip; and

encapsulation material encapsulating said semiconductor chip, said plurality of conductive wires, said chip paddle, and said plurality of internal leads to form a package body;

wherein said chip paddle has a plurality of through-holes in said half-etched section of said chip paddle for increasing the bonding strength of said encapsulation material in said package body; and

wherein said chip paddle has a plurality of through-holes in said half-etched section of said chip paddle for increasing the bonding strength of said encapsulation material in said package body.

16. The packaged semiconductor of claim 15, wherein said chip paddle has a perimeter and said half-etched section is located at a lower edge of said chip paddle along said chip paddle perimeter.

17. The packaged semiconductor of claim 15, wherein said plurality of tie bars each has a side surface and a bottom surface.

18. The packaged semiconductor of claim 15, wherein each of said plurality of tie bars externally extend and has a half-etched section.